Chapter 8
Formal Verification of Real-time Systems

Real-Time Embedded Systems Laboratory
Northeastern University

Comparison

- Three methods for system property validation
  - Model Checking (Automatic Formal Verification)
  - Simulation & Testing
  - Theorem Proving

Simulation & Testing

- Basic procedure
  - take model (simulation) or realization (testing)
  - stimulate it with certain inputs, i.e., test cases
  - observe produced behavior and check whether this is ”desired”
- Benefits
  - Easy to do
  - More efficient than Formal Verification
- Problems:
  - unexplored behaviors may contain fatal bugs

(Testing and simulation can show the presence of bus, not their absence)

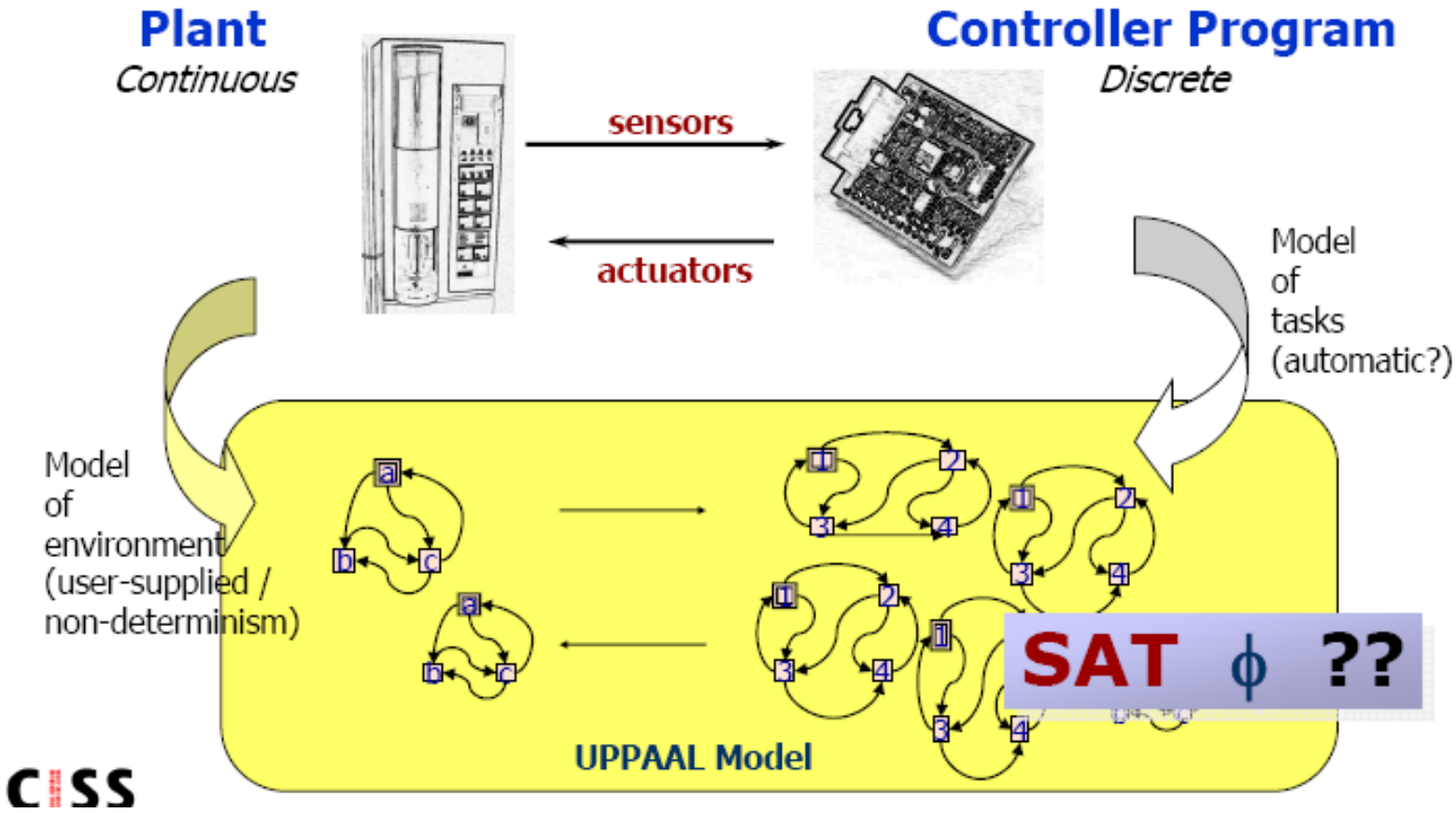
Theorem Proving

- Basic procedure
  - describe the system as a mathematical theory
  - express the property in the mathematical theory
  - prove that the property is a theorem in the mathematical theory
- Benefits:
  - efficient
  - difficult
    - express the system as a mathematical theory, and find its proof
  - pessimistic

Model-checking

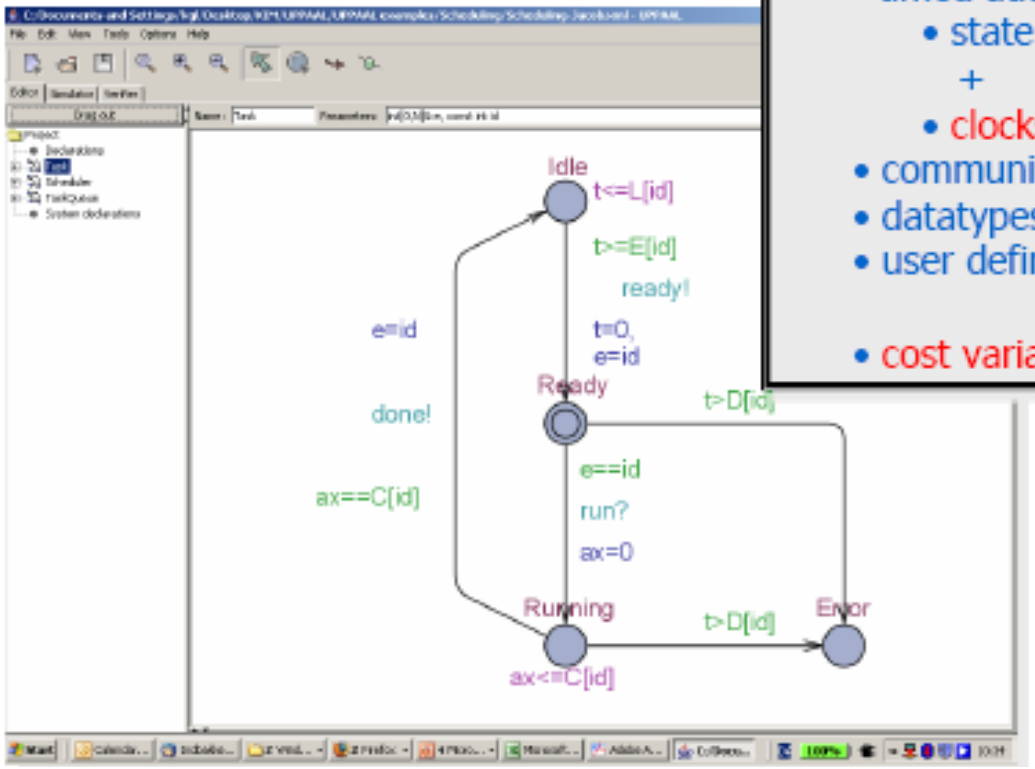
- Basic procedure:
  - describe the system as finite state model
  - express properties in Temporal Logic
  - formal verification by automatic exhaustive search over the state space
- Benefits:
  - Exact (abstract) specification
  - Exhaustively analysis of the formal specification
- Problems
  - Could be too time and memory consuming
  - Difficult to do

Model-checking



A Model Checker for Real-time Systems

UPPAAL

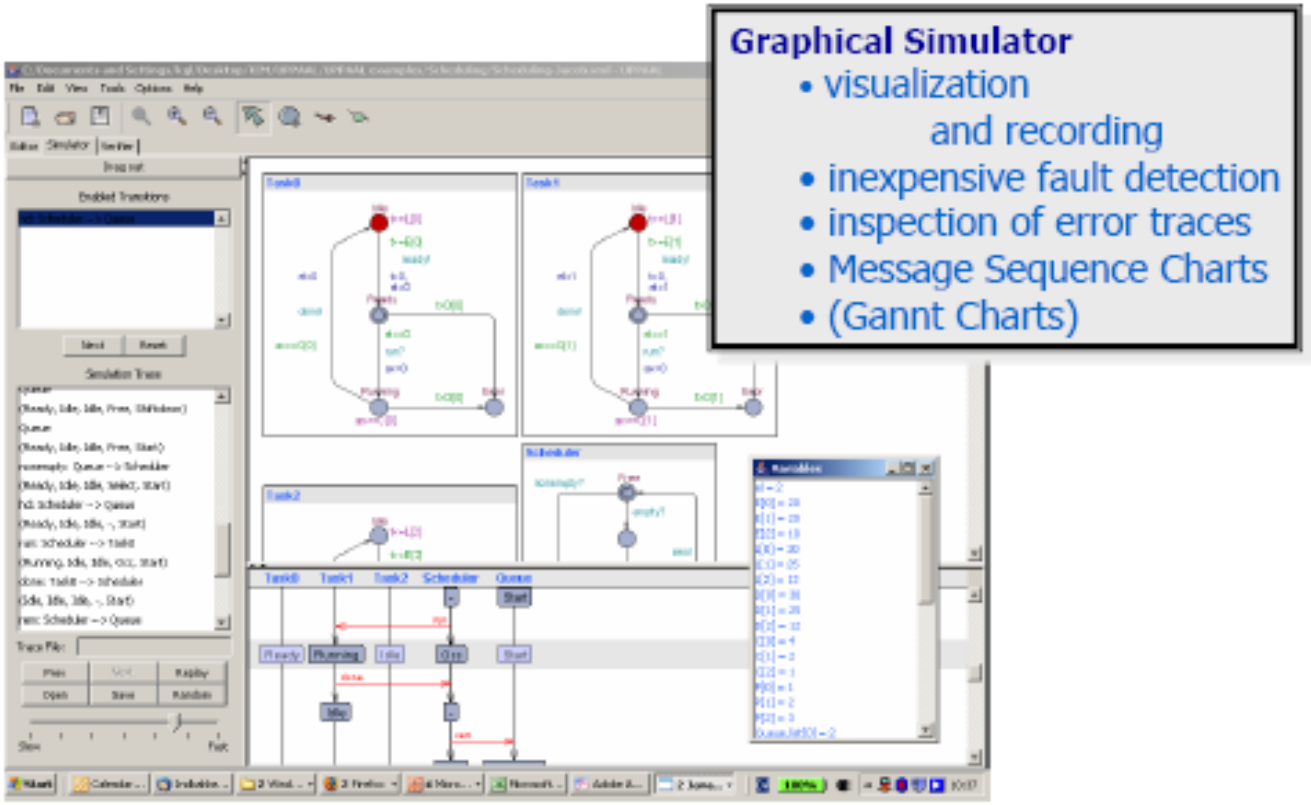


Graphical Design Tool

- timed automata =
  - state machines
    +
  - clocks
- communication
- datatypes
- user defined functions

- cost variable

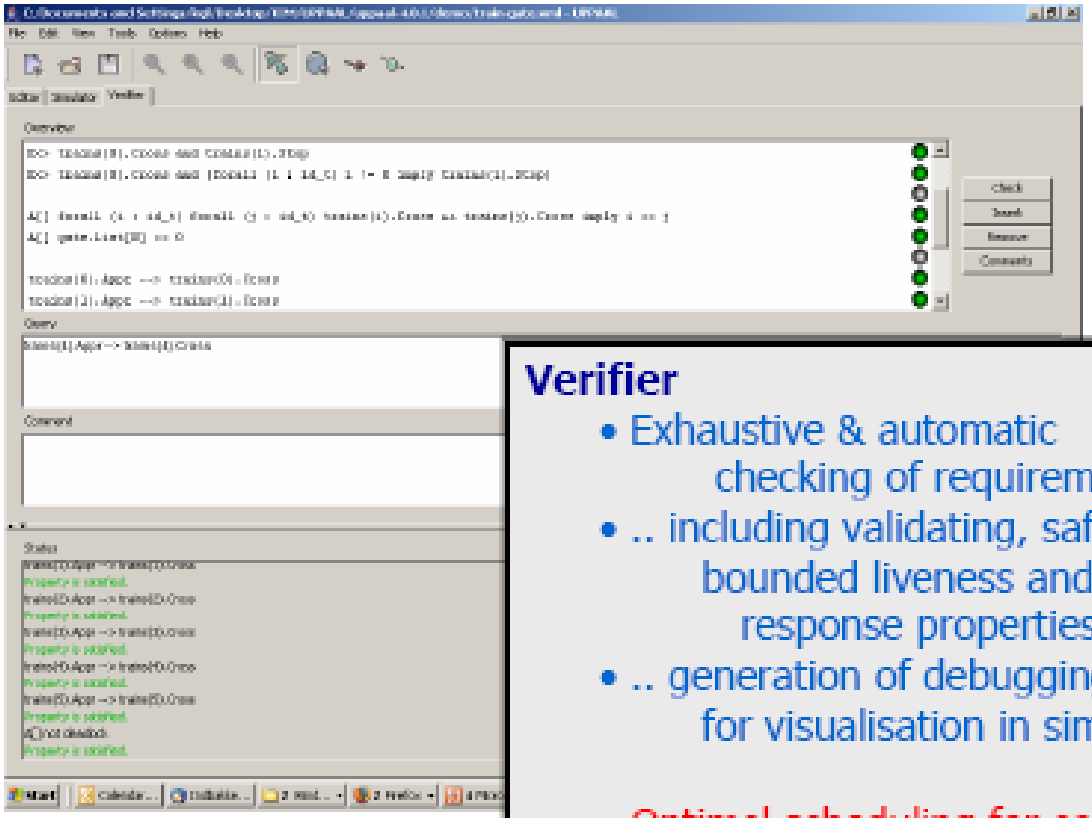
UPPAAL



Graphical Simulator

- visualization and recording
- inexpensive fault detection
- inspection of error traces
- Message Sequence Charts
- (Gannt Charts)

UPPAAL

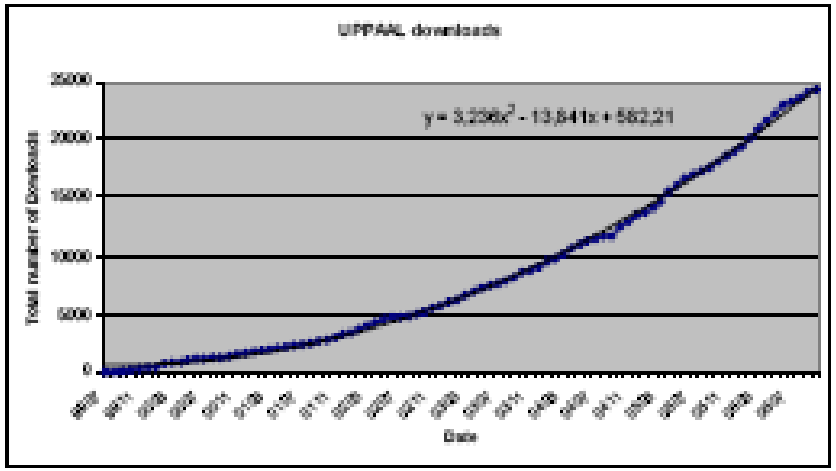


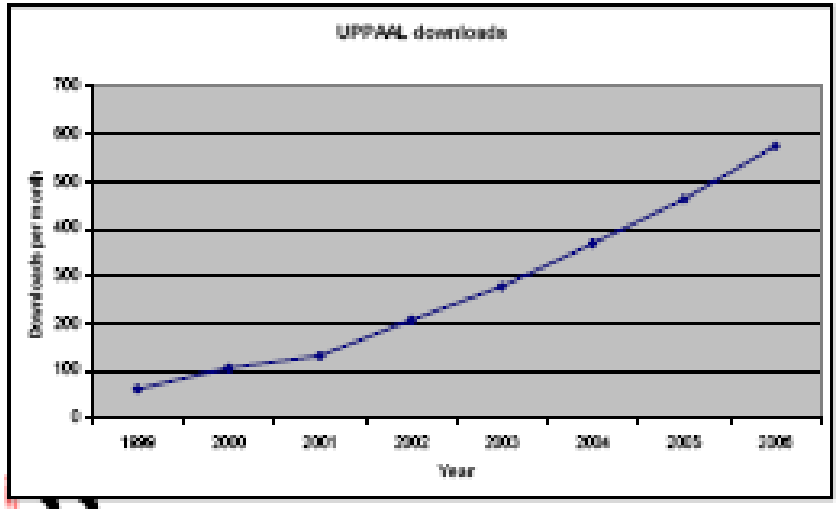
Verifier

- Exhaustive & automatic checking of requirements
- .. including validating, safety, liveness, bounded liveness and response properties
- .. generation of debugging information for visualisation in simulator.

- Optimal scheduling for cost models

Impact





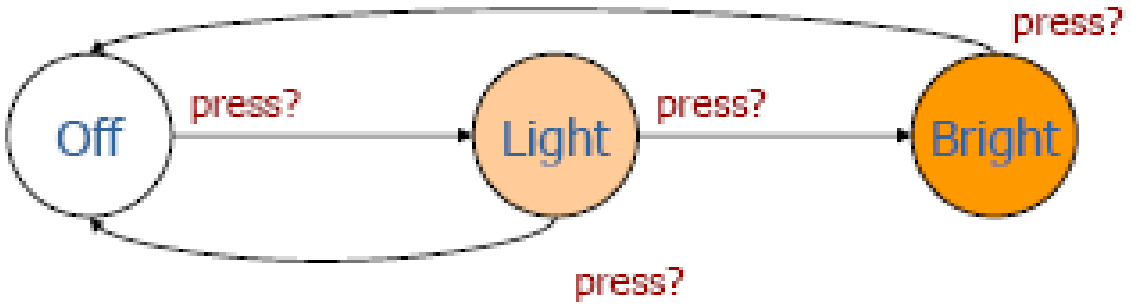
Google:

UPPAAL:	134.000
SPIN Verifier:	242.000
nuSMV:	57.700

> 1.500
Google Scholar Citations
(Rhapsody/Esterel < 3.500)

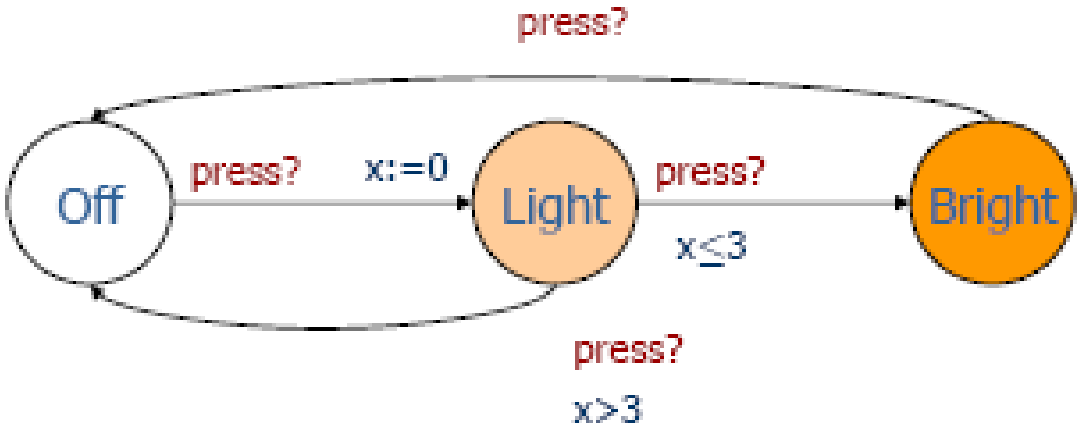
Timed Automata (TA)

Dumb Light Control



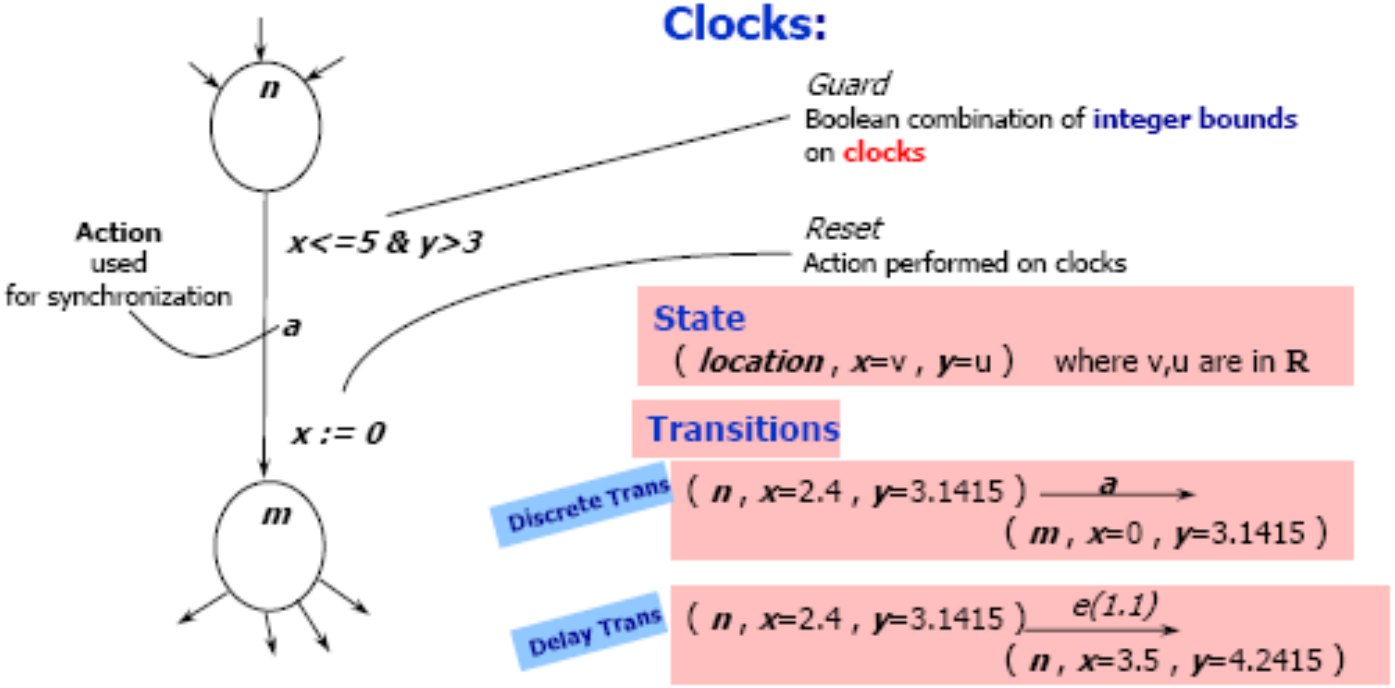
WANT: if press is issued twice quickly
then the light will get brighter; otherwise the light is turned off.

Dumb Light Control

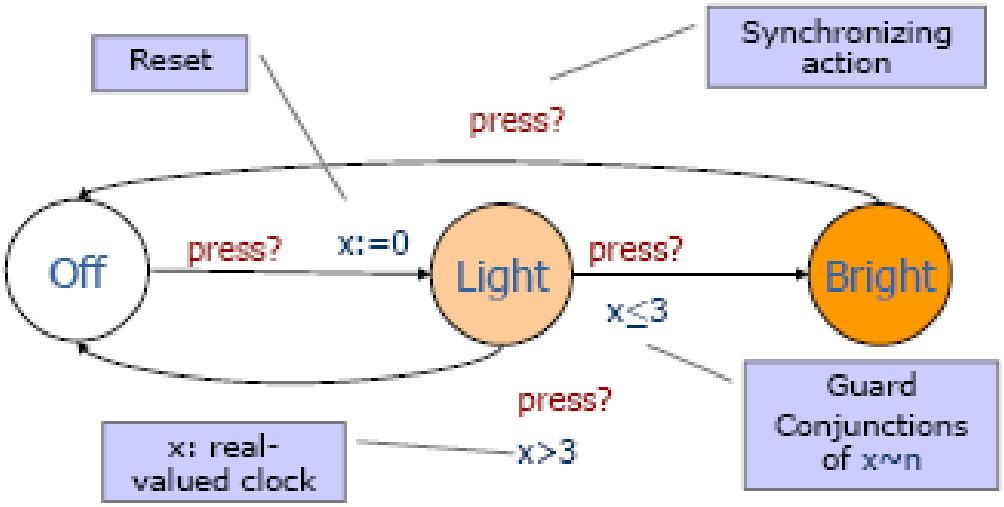


Solution: Add real-valued clock **x**

Timed Automata



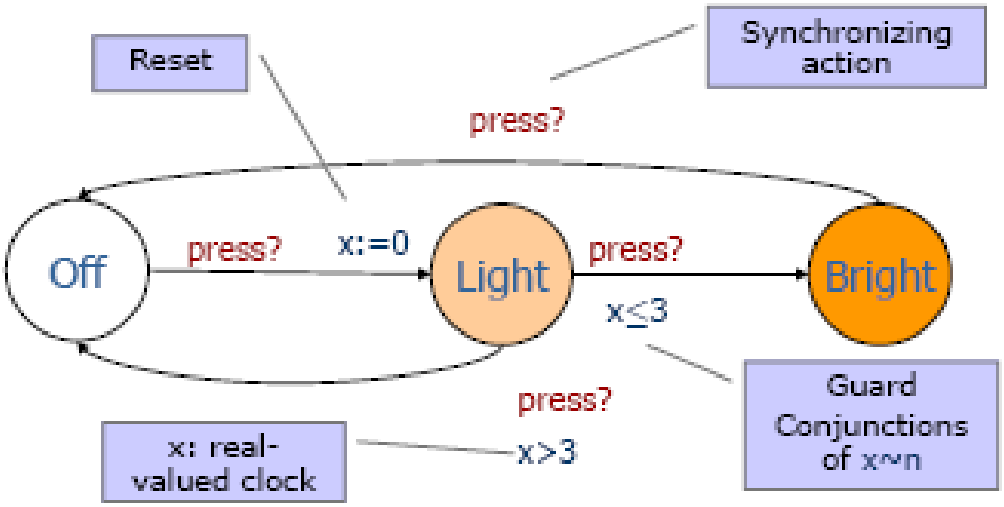
Timed Automata



States:
(location , x=v) where v∈**R**

Transitions:
(Off , x=0)

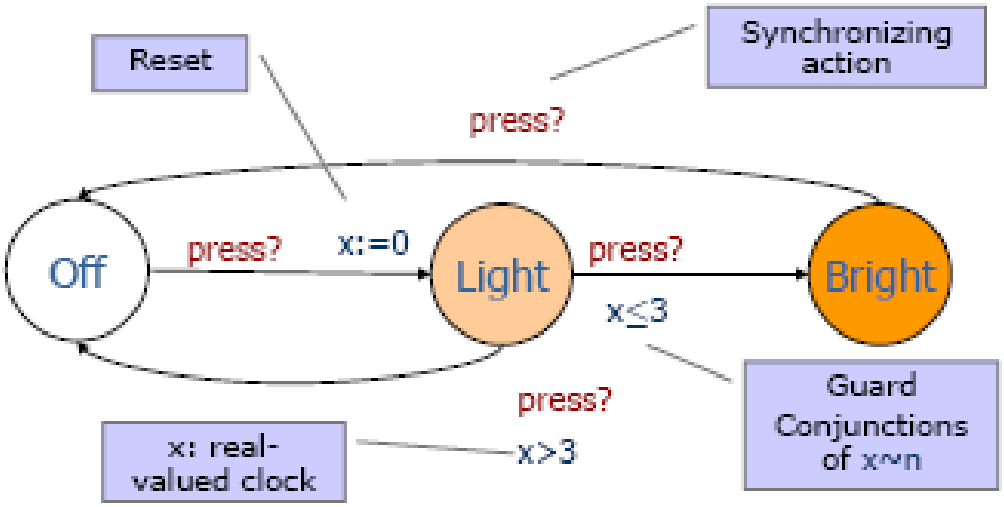
Timed Automata



States:
(location , x=v) where v∈**R**

Transitions:
(Off , x=0)
delay 4.32 → (Off , x=4.32)

Timed Automata

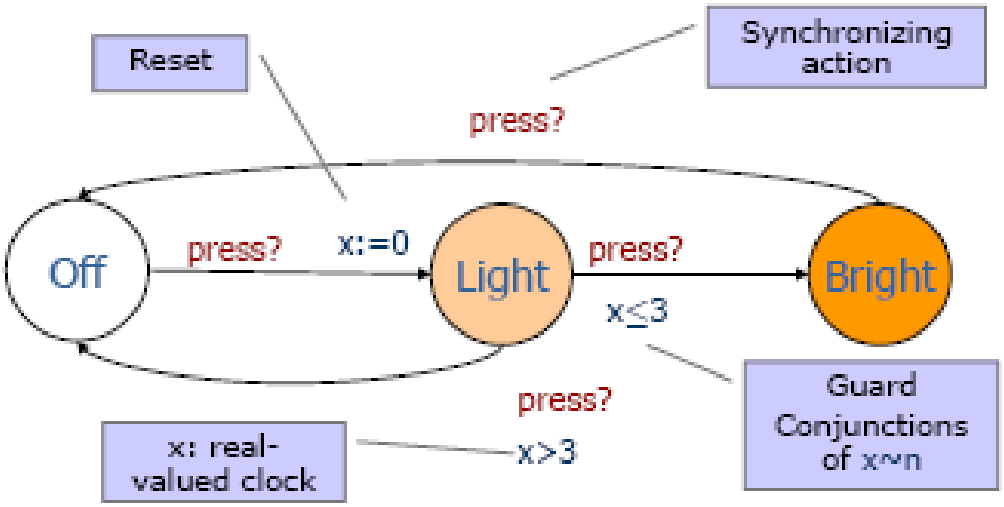


States:
(location , x=v) where v∈**R**

Transitions:

(Off , x=0)
delay 4.32 → (Off , x=4.32)
press? → (Light , x=0)

Timed Automata



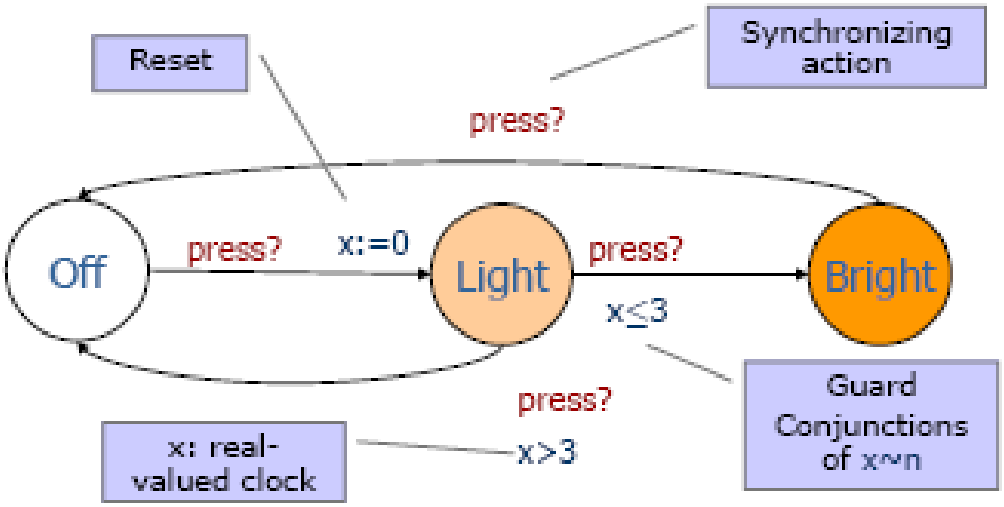
States:
(location , x=v) where v∈**R**

Transitions:

(Off , x=0)

delay 4.32	→ (Off , x=4.32)
press?	→ (Light , x=0)
delay 2.51	→ (Light , x=2.51)

Timed Automata

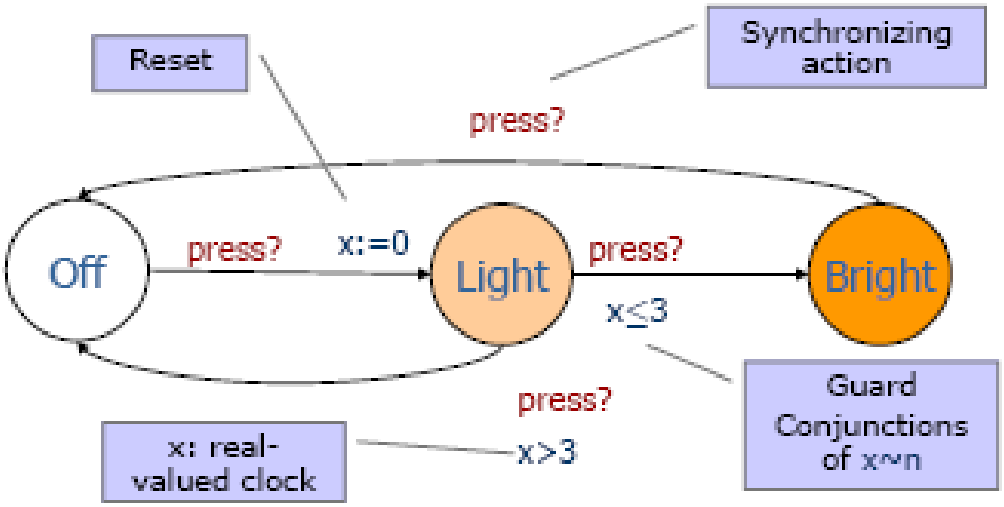


States:
(location , x=v) where v∈**R**

Transitions:

	(Off , x=0)
delay 4.32	→ (Off , x=4.32)
press?	→ (Light , x=0)
delay 2.51	→ (Light , x=2.51)
press?	→ (Bright , x=2.51)

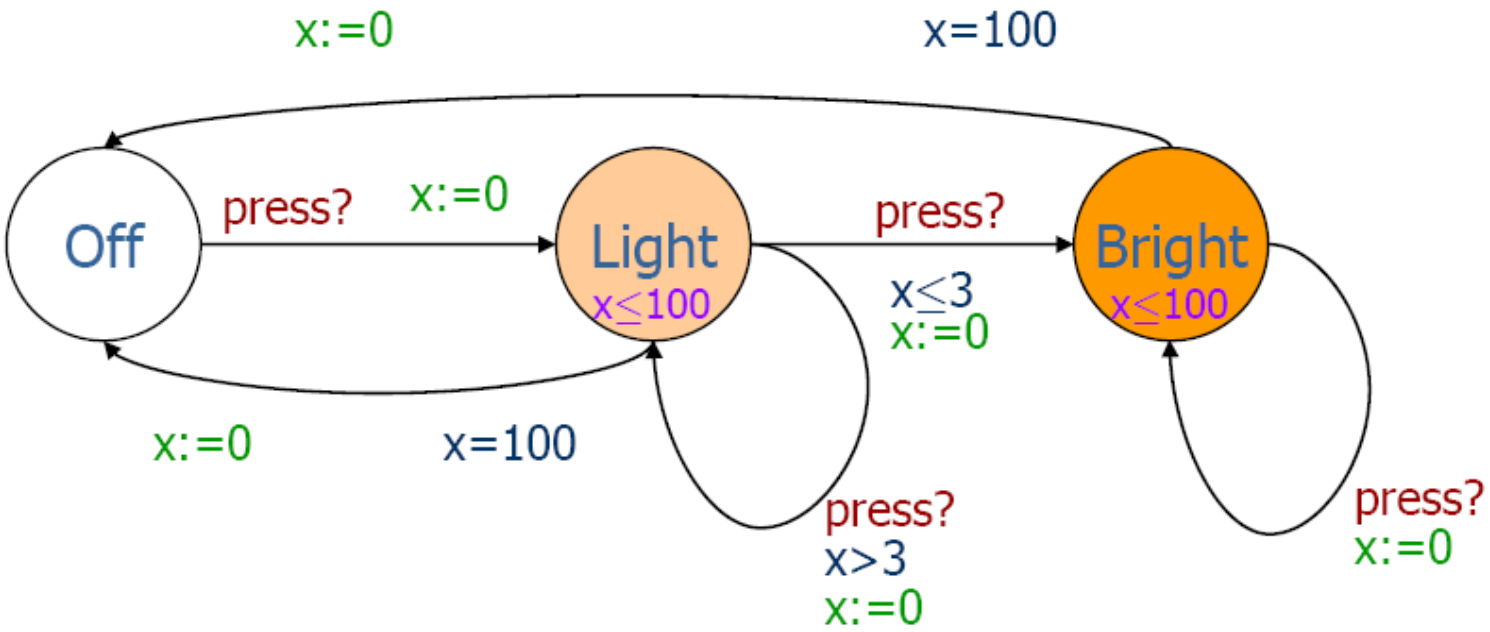
Timed Automata

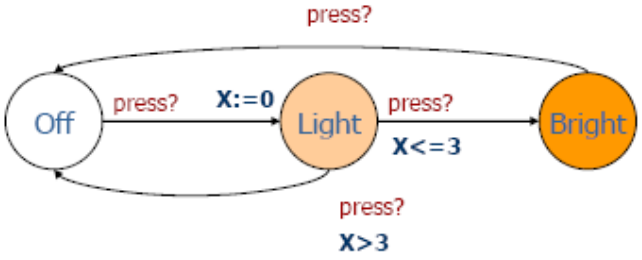


States:
(location , x=v) where v∈**R**

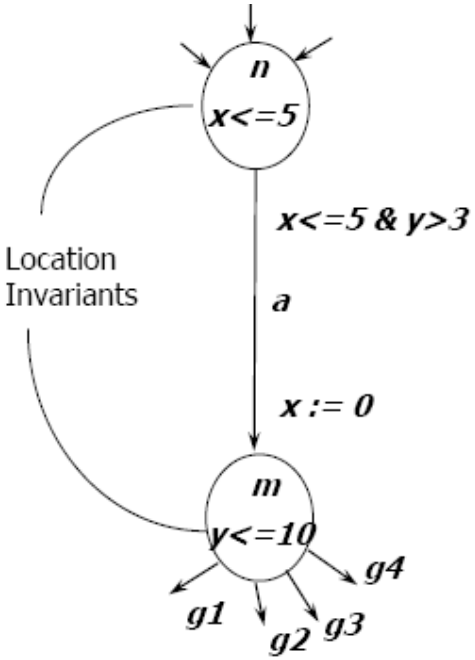
Transitions:
(Off , x=0)

Intelligent Light Control





Invariant



Clocks: *x, y*

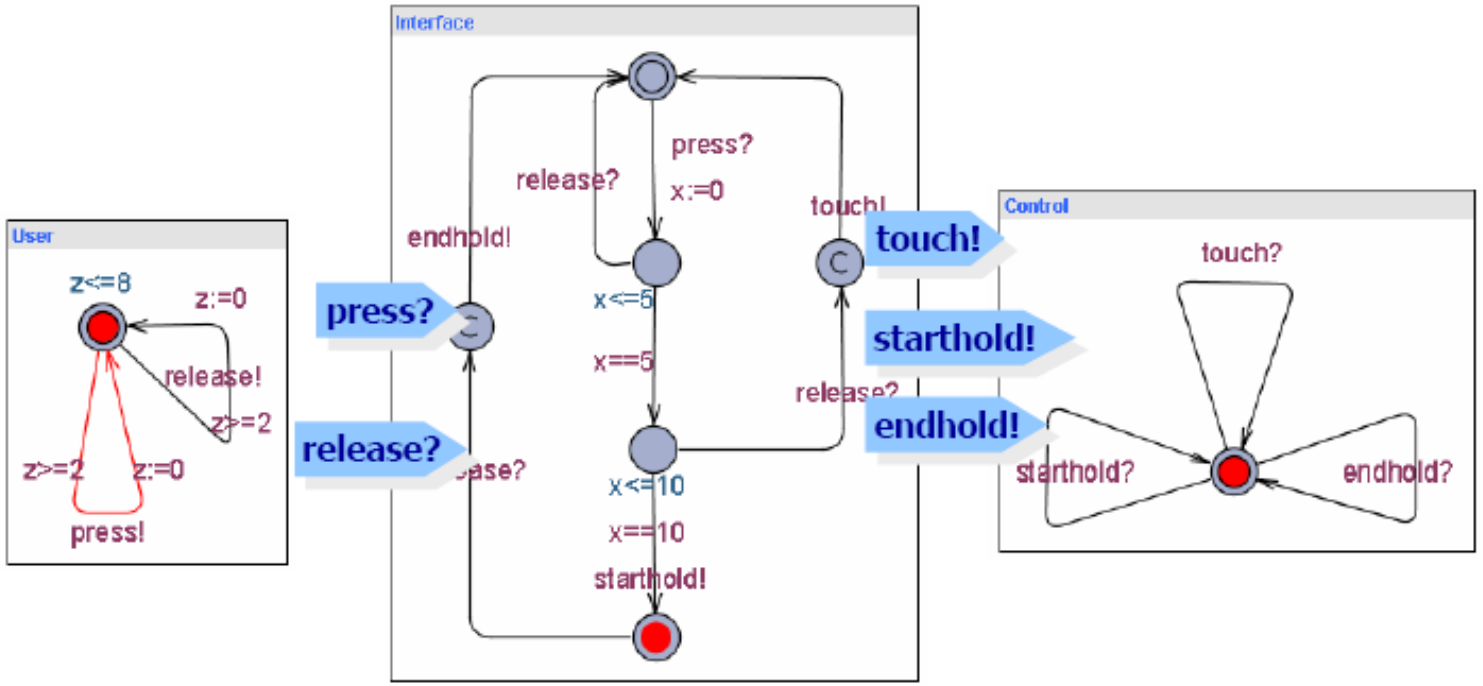
Transitions

(*n* , *x*=2.4 , *y*=3.1415) —e(3.2)→ ✗

(*n* , *x*=2.4 , *y*=3.1415) —e(1.1)→ (*n* , *x*=3.5 , *y*=4.2415)

Invariants ensure progress!!

Composition of TAs



Declarations in UPPAAL

The syntax used for declarations in UPPAAL is similar to the syntax used in the C programming language.

Clocks:

- Syntax:

```
clock x1, …, xn ;
```

- Example:
- `clock x, y;` **Declares two clocks: x and y.**

Declarations in UPPAAL

Data variables

- Syntax:

```
int n1, … ;
int[l,u] n1, … ;
int n1[m], … ;
```

Integer with "default" domain.

Integer with domain "l" to "u".

Integer array w. elements n1[0] to n1[m-1].

- Example:

```
int a, b;
int[0,1] a, b[5][6];
```

Declarations in UPPAAL

Actions (or channels):

- Syntax:

```
chan a, … ;
urgent chan b, … ;
```

Ordinary channels.
Urgent actions (see later)

- Example:

```
chan a, b;
urgent chan c;
```

Declarations in UPPAAL

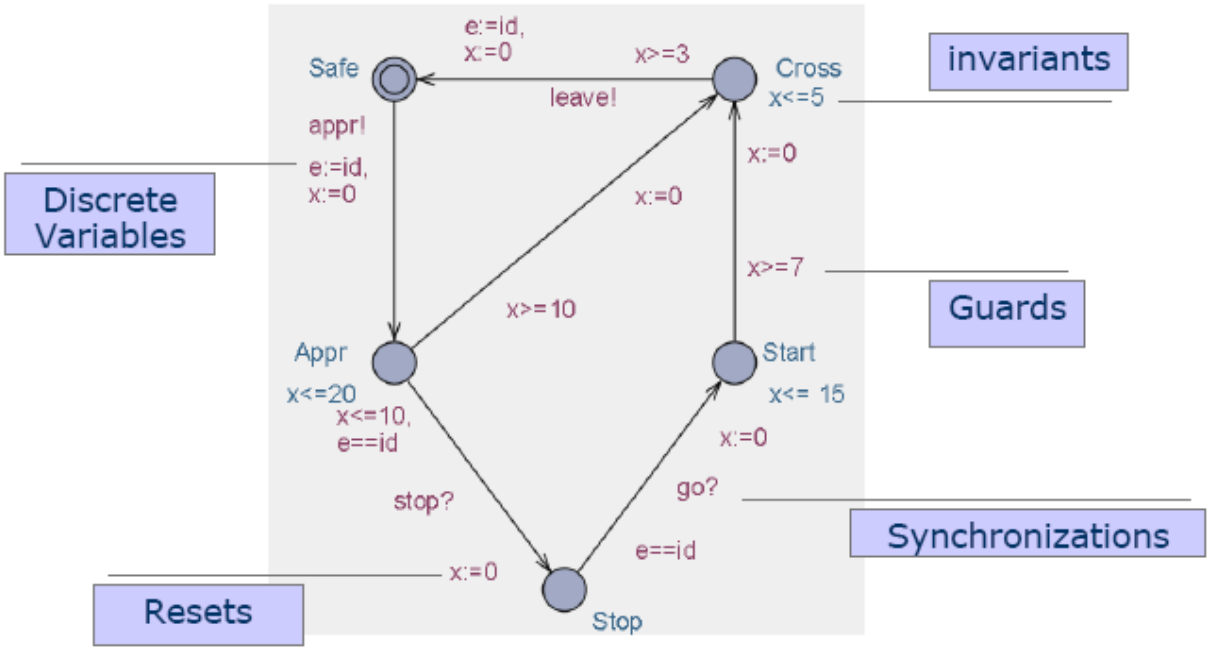
Constants

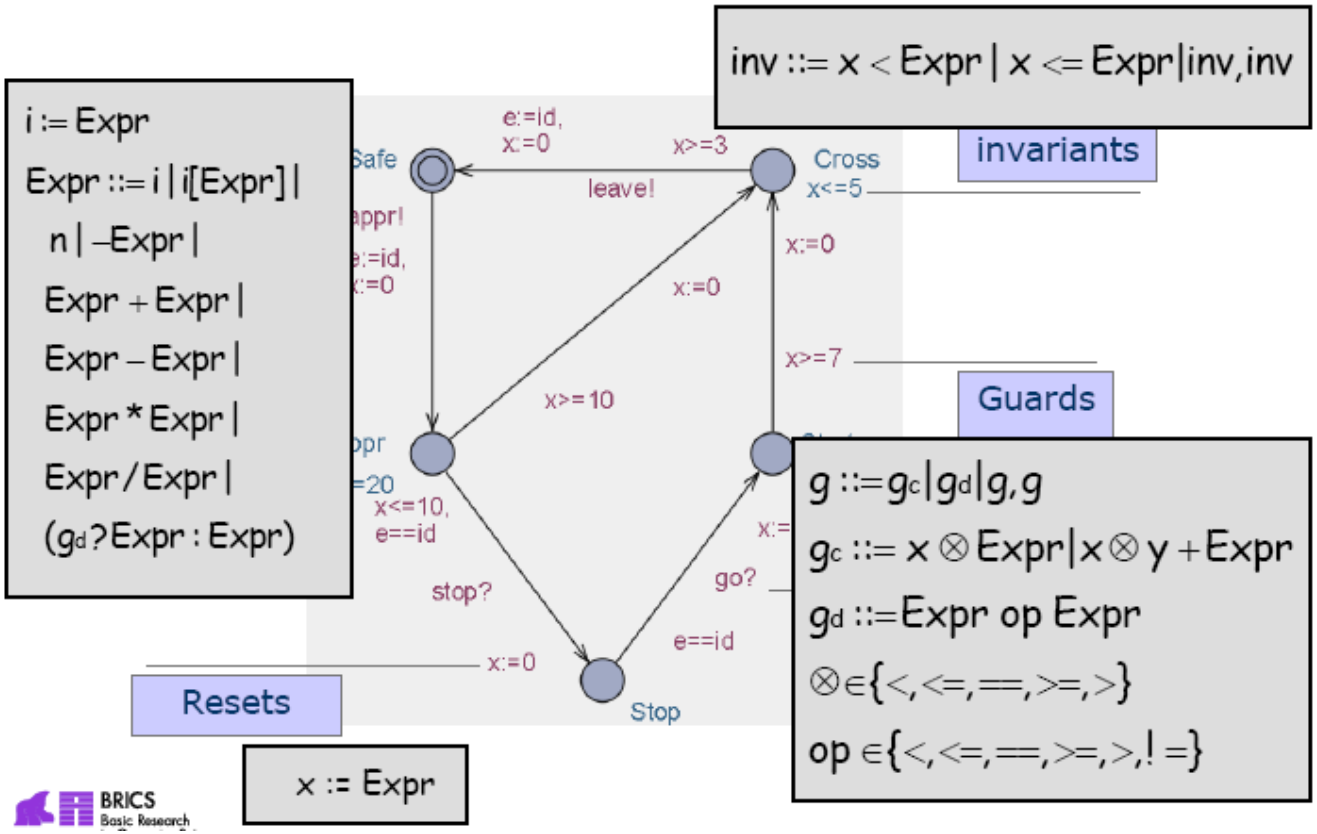
- Syntax:

```
const int c1 = n1;
```

- Example:
- `const int[0,1] YES = 1;`
- `const bool NO = false;`

Timed Automata in UPPAAL




i := Expr
Expr ::= i | i[Expr] |
n | –Expr |
Expr + Expr |
Expr – Expr |
Expr * Expr |
Expr / Expr |
(gd ? Expr : Expr)
inv ::= x < Expr | x <= Expr|inv,inv
invariants
Guards
g ::= gc|gd|g,g
gc ::= x ⊗ Expr|x ⊗ y + Expr
gd ::=Expr op Expr
⊗∈{<,<=,==,>=,>}
op ∈{<,<=,==,>=,>,! =}
Resets
x := Expr
Safe
Cross
Stop
e:=id,
x:=0
x>=3
leave!
x<=5
x:=0
x:=0
x>=7
x>=10
x<=10,
e==id
stop?
go?
e==id
x:=0

Logical Specifications

- Validation Properties
  - Possibly: E<> *P*
- Safety Properties
  - Invariant: A[] *P*
  - Pos. Inv.: E[] *P*
- Liveness Properties
  - Eventually: A<> *P*
  - Leadsto: $P \rightarrow Q$
- Bounded Liveness
  - Leads to within: $P \rightarrow_{\leq t} Q$

The expressions *P* and *Q* must be type safe, side effect free, and evaluate to a boolean.

Only references to integer variables, constants, clocks, and locations are allowed (and arrays of these).

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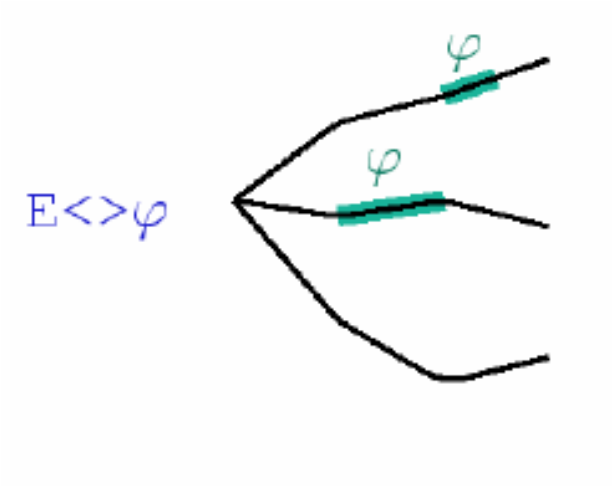

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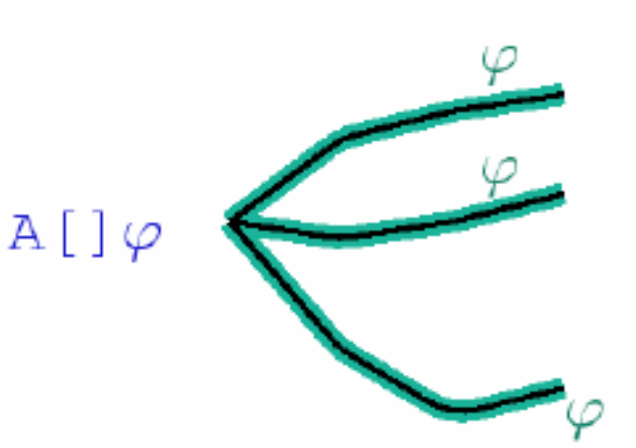

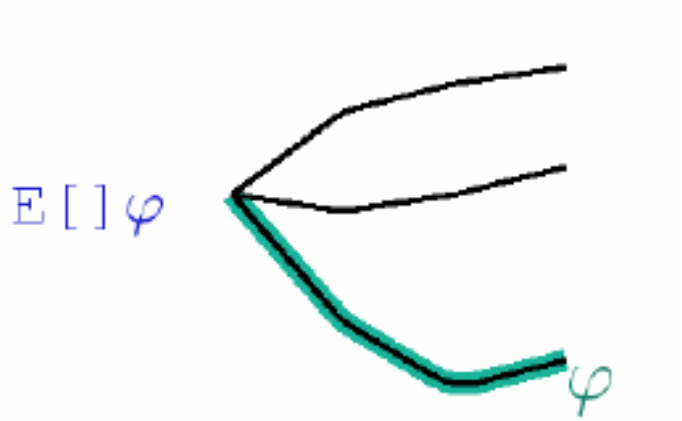

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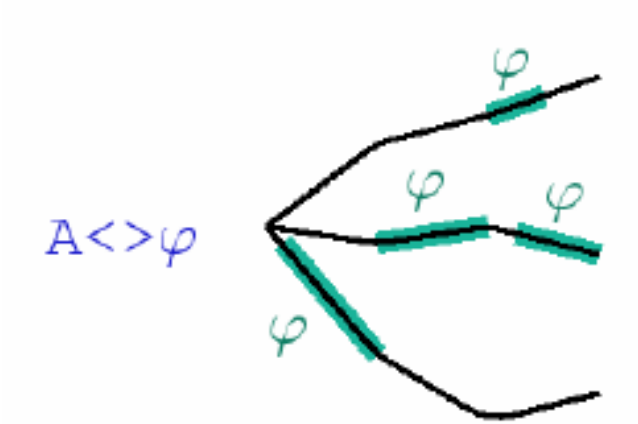

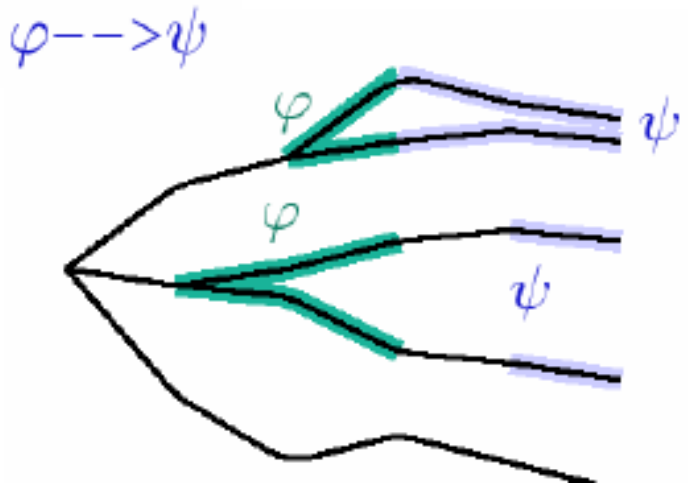

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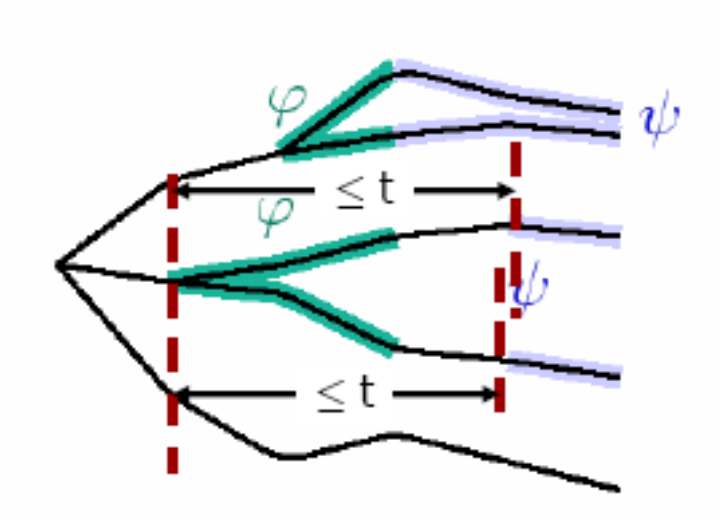

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